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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,335	12/14/2006	Katsuki Kusunoki	Q79257	6238
23373	7590	06/24/2009	EXAMINER	
SUGHRUE MION, PLLC			PATHAK, SHANTANU	
2100 PENNSYLVANIA AVENUE, N.W.				
SUITE 800			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20037			2829	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/581,335	KUSUNOKI, KATSUKI	
	<b>Examiner</b>	<b>Art Unit</b>	
	SHANTANU C. PATHAK	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 18 May 2009.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-11 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-11 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.  
 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_.  
 5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_.

**DETAILED ACTION**

1. Claims 1-11 are pending in the instant application.

***Response to Arguments***

2. Applicant's arguments, filed in an amendment dated May 18<sup>th</sup>, 2009 with respect to the rejection(s) of Claim(s) 1, 3-11 under 35 U.S.C. 103(a) have been fully considered and are not persuasive. The rejection of Claim(s) 1, 3-11 stand.

In response to the argument, "...First, Shuji teaches away from the offset center lines of Araghi...", the examiner respectfully disagrees. Shuji cannot teach away from a feature that it does not disclose (i.e. slanted center lines). Though Shuji enables using perpendicular center lines, it makes no mention that slanted center lines cannot be used for making slanted fracture lines.

In response to the argument, "...Further, Shuji teaches away from separating the chips along slanted lines since Shuji teaches that when the thickness of the wafer is too thick, the fracture line may become slanted as shown along line c in Drawing 1 ([0010])...", the examiner respectfully disagrees. Line 'c' is a fracture line resultant from a perpendicular center line. It is obvious that the intended fracture line for a perpendicular center line is a perpendicular fracture line. The intended fracture line for a slanted center line is a slanted fracture line. Hence the combination of Shuji with Araghi.

In response to the argument, "...Second, a skilled artisan would not have been motivated to precisely control the ends and line edges of Shuji for butting against the ends of arrays as in

Araghi...Accordingly, a skilled artisan would not have been motivated to abut the light emitting devices of Shuji as asserted by the Examiner...”, the examiner respectfully disagrees. The benefit is disclosed in Araghi, therein providing a reason to combine Shuji with Araghi to achieve the benefit.

In response to the argument, “...Third, with regard to claim 6, the Examiner's interpretation is incorrect... Accordingly, a skilled artisan would not have achieved the features of claim 6 based on the disclosures of Shuji and Araghi, contrary to the Examiner's assertion...”, the examiner respectfully disagrees. As per Fig. 4, Para. 16, the p-type GaN layer 3 is etched in a quarter-circular shape at the position confronting the first grooves (W1) so as to expose the n-type GaN layer 2 and use it as an electrode-forming surface.

In response to the argument, “...It is impossible to combine the method of Araghi, which separates chips by utilizing the cleavability of silicon crystal, with the method of Shuji, which utilizes a sapphire substrate possessing no cleavability...”, the examiner respectfully disagrees. Araghi is being relied upon to teach a second groove formed on a diametrically opposite side of a substrate as the first groove and not conforming to the center lines of the first groove (i.e. that a slanted cutting line is well known in the art). Specific fracture planes are dependent on the sapphire material, which is taught by Shuji. Combining the teaching of Shuji, which includes the sapphire substrate, with the teaching of Araghi, which includes the slanted cutting line, enables one to arrive at the claimed invention of the instant application.

In response to the argument, “...with regard to claim 4, Applicant disputes that Shuji in view of Araghi disclose the general conditions of the rejected claims, as asserted by the Examiner...”, the examiner respectfully disagrees. The examiner agrees that the angle formed

between the (111) plane and the (100) plane is 54.7° and further concedes that neither Shuji nor Araghi explicitly disclose cut faces having angles in the range of 60 to 85°, however it would have been obvious to one of ordinary skill in the art at the time of the invention to test cut face angle ranges between 60 and 85° from a starting cut face angle of 54.7° (i.e. Araghi discloses the general conditions of the cut face angle).

3. Applicant's arguments, filed in an amendment dated May 18<sup>th</sup>, 2009 with respect to the rejection of Claim 2 under 35 U.S.C. 103(a) have been fully considered and are persuasive. The rejection of Claim 2 has been withdrawn.

#### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 3-7, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuji et al. (Japan Patent No. JP10125958), hereinafter referred to as “Shuji”, in view of Araghi (US Patent No. 4,604,161), hereinafter referred to as “Araghi”.

**With respect to Claim 1**, Shuji teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, comprising: a step of linearly forming first grooves in a desired chip shape by etching on a side of the gallium nitride compound semiconductor layers of said wafer (Paragraph 7, lines 1-6; Drawing 3, elements 11, 2, 3); a step of forming second grooves having a line width (W2) equal to or smaller than a line width (W1) of the first grooves on a side of the substrate of said wafer (Paragraph 7, lines 9, 10; Drawing 3, elements W1, 11, W2, 22); and a step of dividing said wafer along said first and second grooves into pieces each of a chip shape (Paragraph 7, lines 11, 12; Paragraph 10, lines 12-14; Paragraph 21, lines 9, 10) {Examiner’s note: The wafers are separated along the “Chuo Line”}.

Shuji does not teach the limitation wherein the second grooves are formed at positions not conforming to the central lines of the first grooves.

Araghi teaches a method of fabricating image sensor arrays for assembly with other like arrays to form a longer composite array without sacrifice of image quality. Araghi further discloses the limitation wherein the second grooves are formed at positions not conforming to the central lines of the first grooves (Column 3, lines 50-56; Fig. 3, elements 35, 37, 40, 44, 45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shuji with the groove positioning as taught by Araghi to provide chips having precisely controlled ends and line edges for butting against the ends of like arrays (Araghi).

**With respect to Claims 3-5**, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. Shuji in view of Araghi does not explicitly disclose: the limitation wherein the positions not conforming to the central lines of said first grooves are, when viewing the substrate in plan[e] view, positions parted by 20 to 100% of the line width (W1) of the first grooves relative to the central lines of the first grooves **[Claim 3]**; the limitation wherein at the step of forming said second grooves, the second grooves are formed so that the obliquely divided chips assume cut faces having angles in the range of 60 to 85° **[Claim 4]**; and the step of polishing the substrate side prior to forming the second grooves to adjust a thickness of the substrate in a range of 60 to 100  $\mu\text{m}$  **[Claim 5]**. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to employ the limitations as described in Claims 3-5 of the instant application in the invention of Shuji in view of Araghi because “[w]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

**With respect to Claim 6**, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. Shuji further teaches the limitation wherein said first grooves are confronted by an electrode-forming surface for forming an electrode for gallium nitride compound semiconductor chips (Para. 16; Fig. 4) {Examiner's note: see explanation above}.

**With respect to Claim 7**, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. Shuji further teaches the limitation wherein said second grooves are formed by at least one method selected from the group consisting of etching, dicing, pulse laser and scribe (Paragraph 9, lines 1-3).

**With respect to Claim 11**, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. That the final product resultant from a method for the production of gallium nitride compound semiconductor chips is a gallium nitride compound semiconductor chip is inherent to the process.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shuji in view of Araghi as applied to Claim 1 above, and further in view of Tsuda et al. (US PG Pub No. 2002/0014681 A1), hereinafter referred to as “Tsuda” and Yamasaki (US PG Pub No. 2002/0105986 A1), hereinafter referred to as “Yamasaki”.

**With respect to Claim 2,** Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. Shuji in view of Araghi does not teach the limitation wherein said substrate is formed of sapphire, with a C surface of the sapphire substrate as the principal surface, said first and second grooves are formed respectively along a first direction parallel to an orientation flat and along a second direction orthogonal to said first direction, and the wafer is divided along the first and second grooves.

Tsuda teaches a method of producing a nitride semiconductor structure for employing in light-emitting devices. Tsuda further discloses the limitation wherein said substrate is formed of sapphire, with a C surface of the sapphire substrate as the principal surface (Para. 57).

Yamasaki teaches a semiconductor laser device formed by a gallium nitride-based semiconductor. Yamasaki further discloses the limitation said first, 32, and second, 34, grooves are formed respectively along a first direction parallel to an orientation flat and along a second direction orthogonal to said first direction, and the wafer is divided along the first and second grooves (Paras. 86-92; Figs. 3-5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shuji in view of Araghi with the substrate as taught by Tsuda and with the grooves as taught by Yamasaki to allow the growth of crystal structure on the substrate (Tsuda: Abstract) and to divide a wafer in accordance with forming a semiconductor laser device (Yamasaki: Para. 93), respectively.

5. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuji in view of Araghi as applied to Claim 1 above, and further in view of Tanaka et al. (US PG Pub No. 2001/0038655 A1), hereinafter referred to as “Tanaka”.

**With respect to Claims 8-10**, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate formed of hexagonal crystal, as described in Claim 1. While Shuji in view of Araghi does not disclose: the limitation wherein said substrate is formed of hexagonal SiC **[Claim 8]**, the limitation wherein said substrate is formed of a hexagonal nitride semiconductor **[Claim 9]**, and the limitation wherein said substrate is formed of hexagonal GaN **[Claim 10]**, the limitations as disclosed in Claims 8-10 are considered as obvious variants.

Tanaka teaches a method of crystal growth of a III-V compound semiconductor composed of at least one group-III element, with the crystal being hexagonal in structure or a nitride semiconductor. Tanaka further discloses the similarities in crystal structure between sapphire and hexagonal SiC (Paragraph 138) **[Claim 8]**, hexagonal nitride semiconductor

(Paragraph 19, lines 11-14) **[Claim 9]** and hexagonal GaN (Paragraph 19, lines 1-10) **[Claim 10]**. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shuji in view of Araghi with the material surfaces as taught by Tanaka to understand crystal growth mechanisms of III-V compound layers for use in semiconductor device applications.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Oohata (US Patent No. 6,963,086 B2), Tanabe et al. (US Patent No. 6,680,959 B2) and Tanabe et al. (US Patent No. 6,735,230 B1) are all related to the manufacture of semiconductor light-emitting devices comprising gallium nitride chips.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHANTANU C. PATHAK whose telephone number is (571) 270-5727. The examiner can normally be reached on Monday-Thursday, 10:00 a.m.-4:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SHANTANU C PATHAK/  
Examiner, Art Unit 2829

/Ha T. Nguyen/  
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